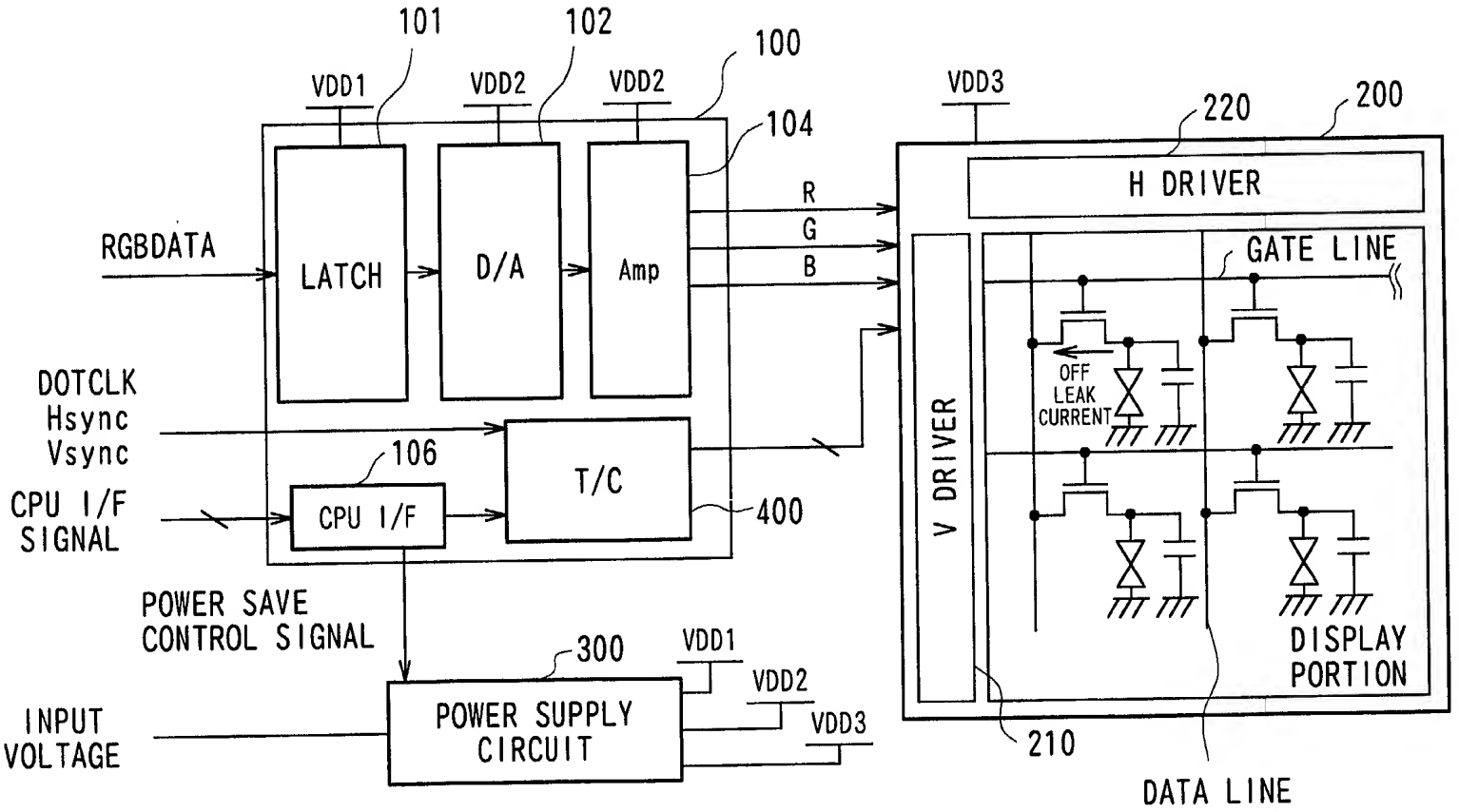

101
102
100
VDD1
VDD2
VDD2
104
VDD3
220
200
H DRIVER
R
G
B
RGBDATA
LATCH
D/A
Amp
GATE LINE
OFF
LEAK
CURRENT
DOTCLK
Hsync
Vsync
106
T/C
CPU I/F
SIGNAL
CPU I/F
400
V DRIVER
POWER SAVE
CONTROL SIGNAL
300
VDD1
VDD2
VDD3
INPUT
VOLTAGE
POWER SUPPLY
CIRCUIT
DISPLAY
PORTION
210
DATA LINE

FIG. 1

FIG. 2 (a)

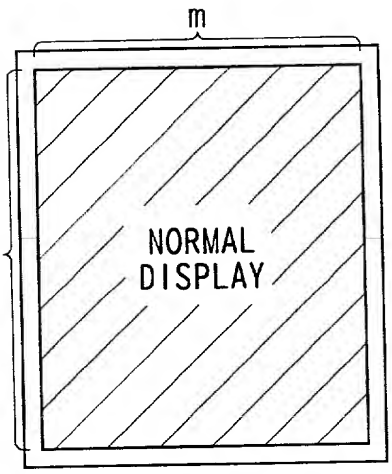


FIG. 2 (b)

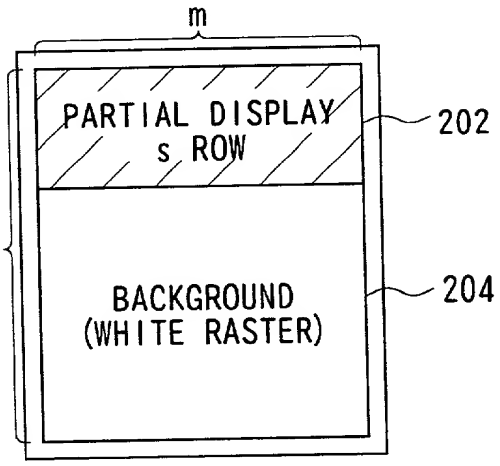
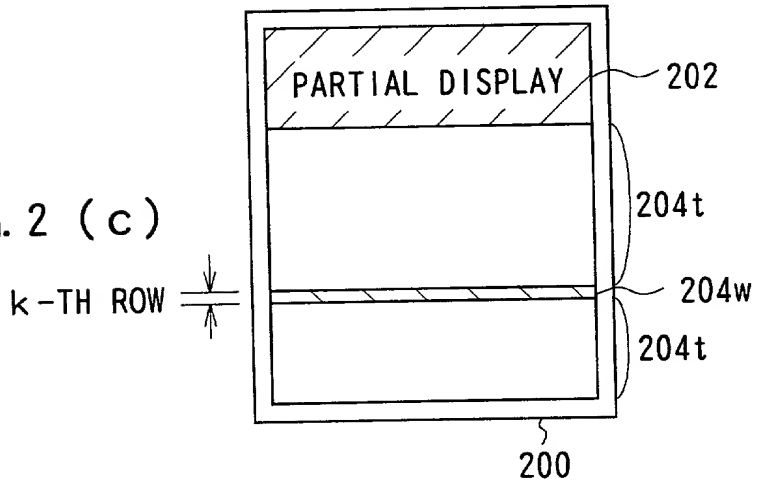


FIG. 2 (c)



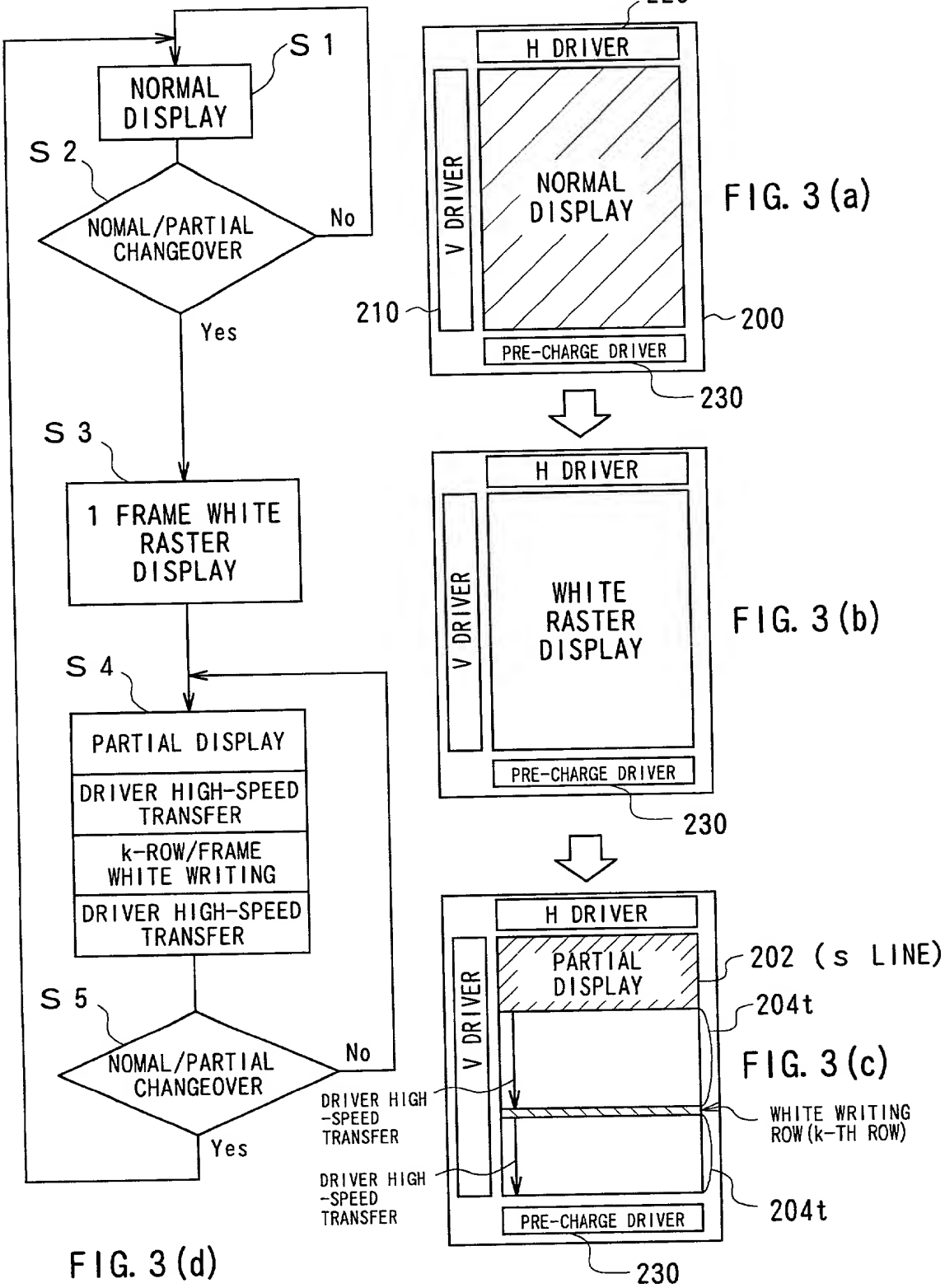


FIG. 3 (a)

FIG. 3 (b)

FIG. 3 (c)

FIG. 3 (d)

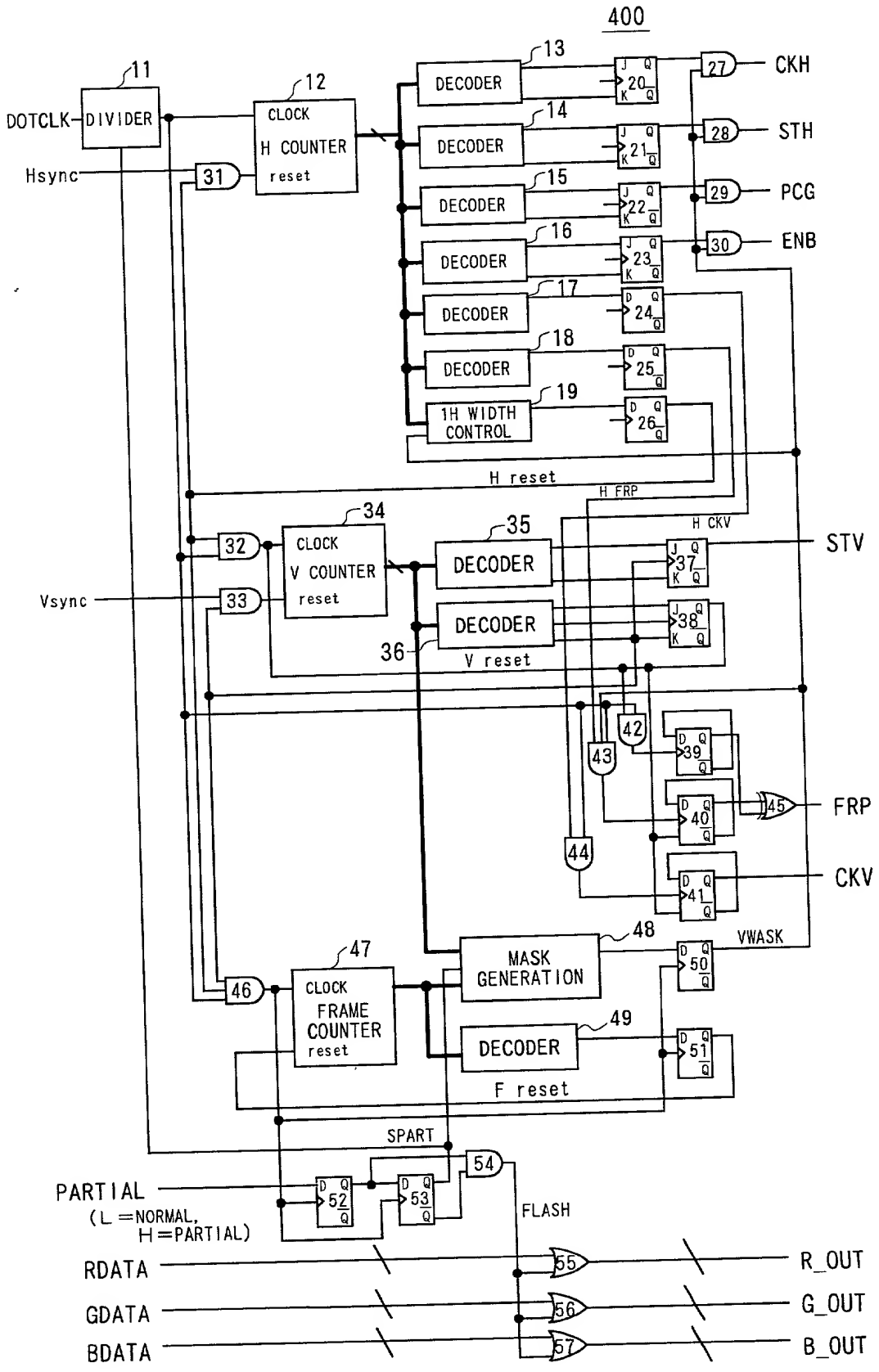

400
11
DIVIDER
DOTCLK
12
CLOCK
H COUNTER
reset
Hsync
31
13
DECODER
14
DECODER
15
DECODER
16
DECODER
17
DECODER
18
DECODER
19
1H WIDTH CONTROL
20
21
22
23
24
25
26
27
CKH
28
STH
29
PCG
30
ENB
H reset
H FRP
H CKV
34
CLOCK
V COUNTER
reset
32
33
Vsync
35
DECODER
DECODER
36
V reset
37
38
STV
42
43
44
39
40
41
45
FRP
CKV
47
CLOCK
FRAME COUNTER
reset
46
MASK GENERATION
48
DECODER
49
F reset
50
51
VWASK
SPART
54
PARTIAL
(L=NORMAL,
H=PARTIAL)
52
53
FLASH
RDATA
GDATA
BDATA
55
56
57
R_OUT
G_OUT
B_OUT

FIG. 4

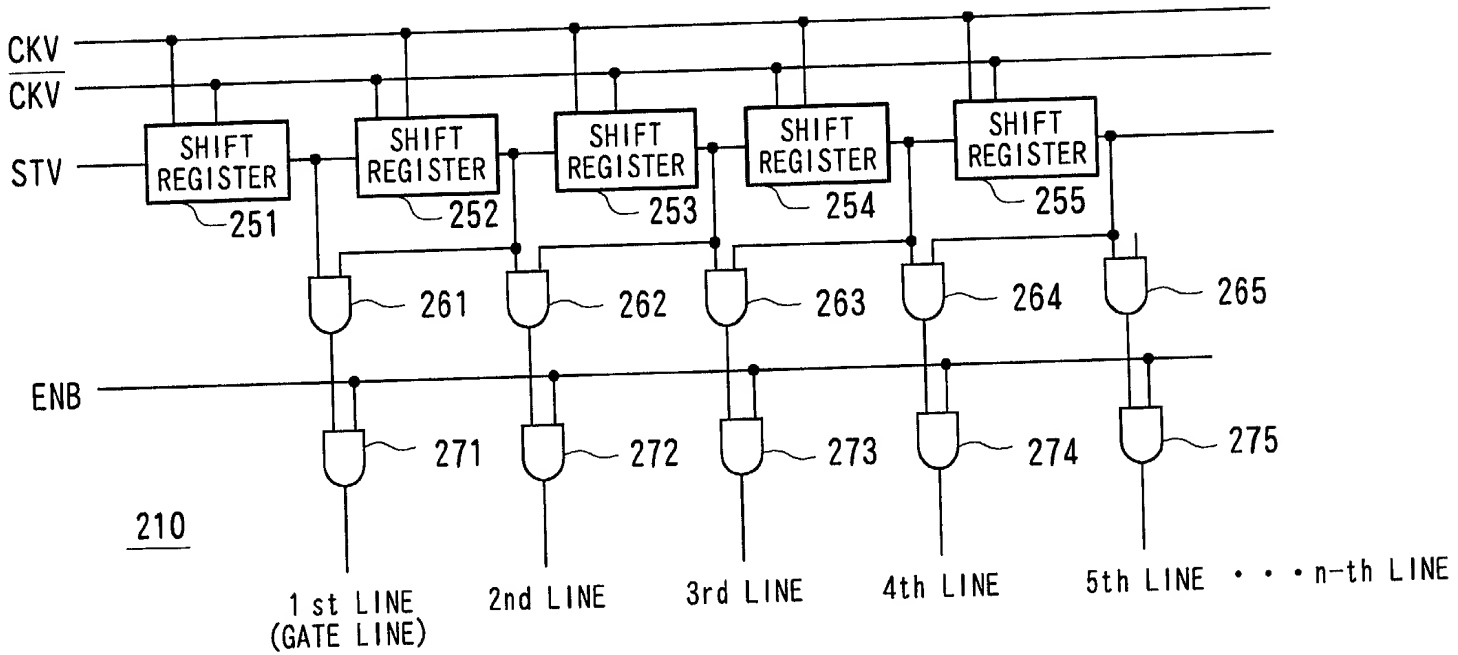

CKV
CKV
STV
SHIFT REGISTER
251
SHIFT REGISTER
252
SHIFT REGISTER
253
SHIFT REGISTER
254
SHIFT REGISTER
255
261
262
263
264
265
ENB
271
272
273
274
275
210
1 st LINE (GATE LINE)
2nd LINE
3rd LINE
4th LINE
5th LINE
• • • n-th LINE

FIG. 5

11:FREQUENCY DIVIDER(DIVIDE-BY-FOUR CIRCUIT)

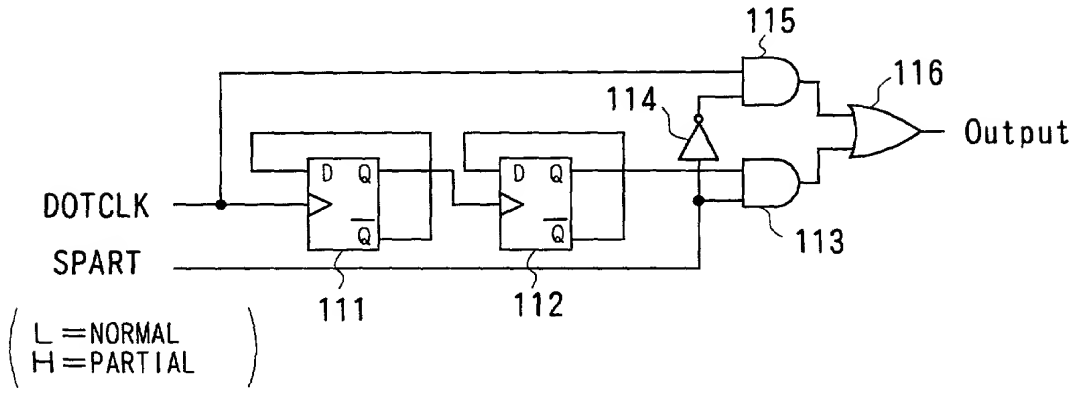
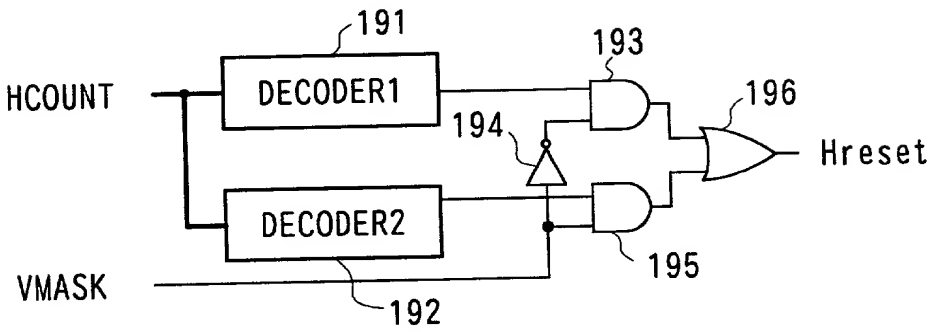


FIG. 6

19:1H WIDTH CONTROL CIRCUIT




```
DECODER1 : if (COUNT=10)    →H
           else             →L
DECODER2 : if (COUNT=120)   →H
           else             →L
```

FIG. 7

48:MASK GENERATOR

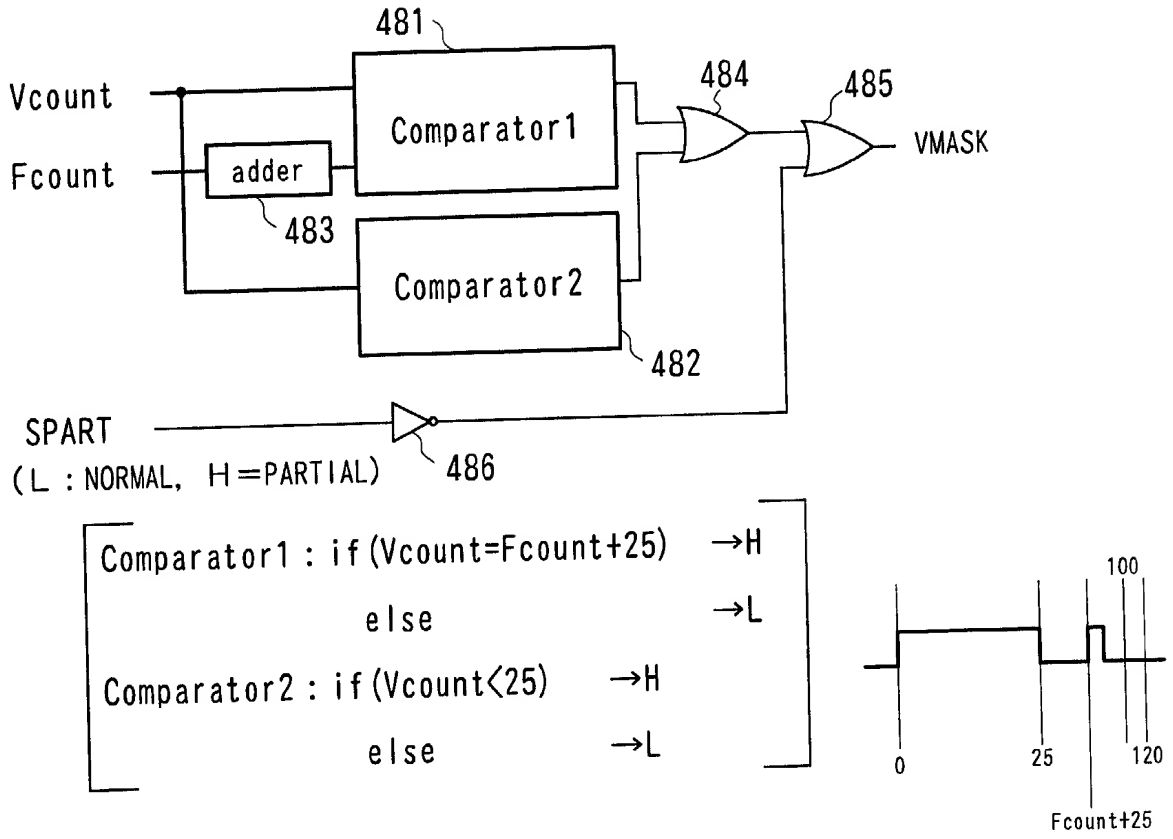
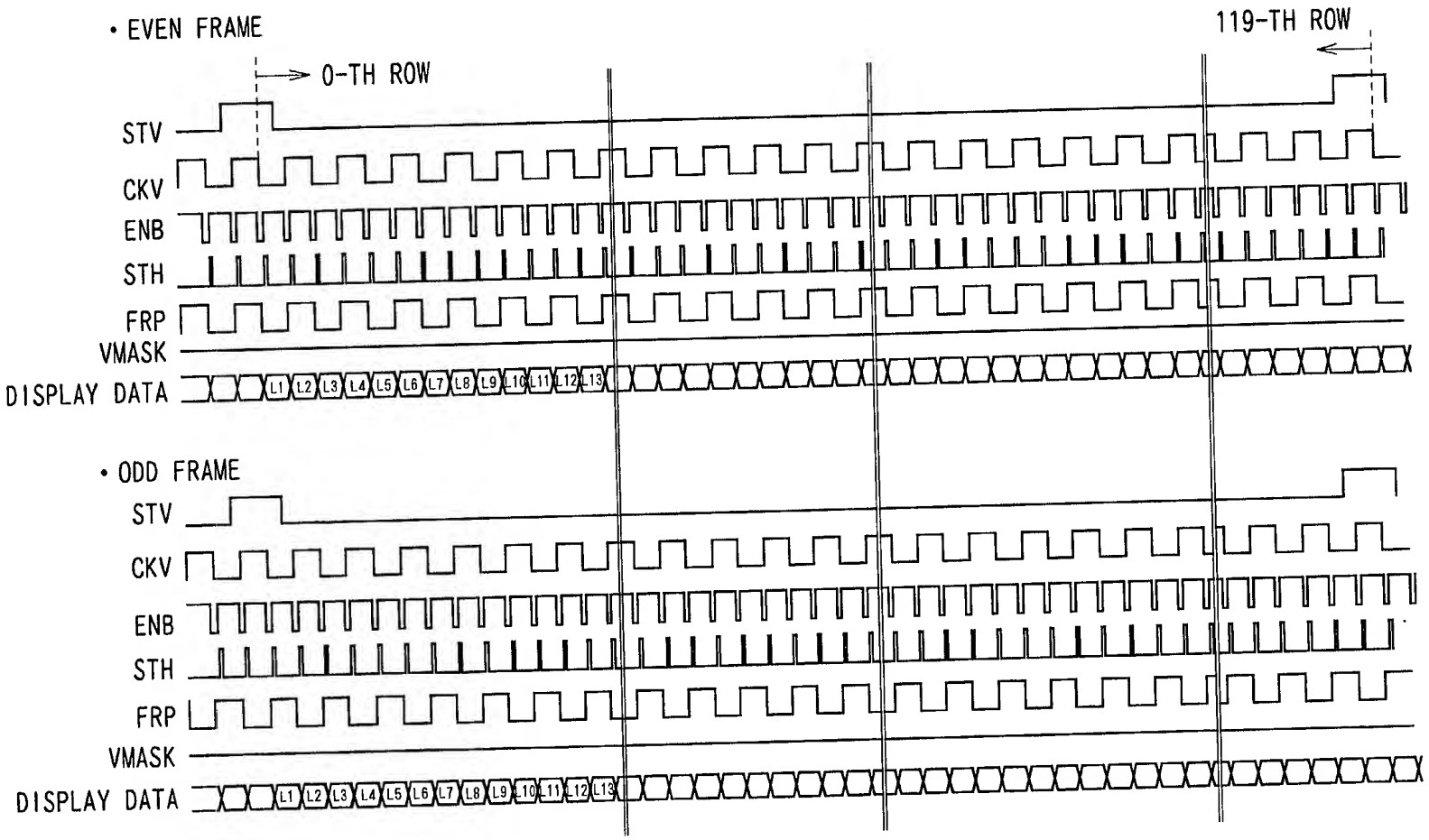


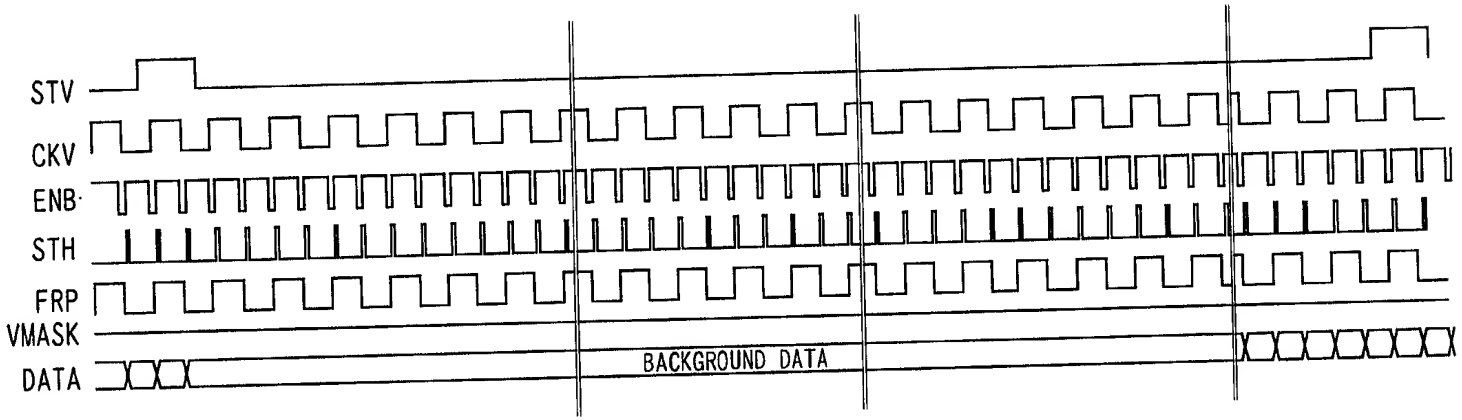
FIG. 8

JP 2007-279680



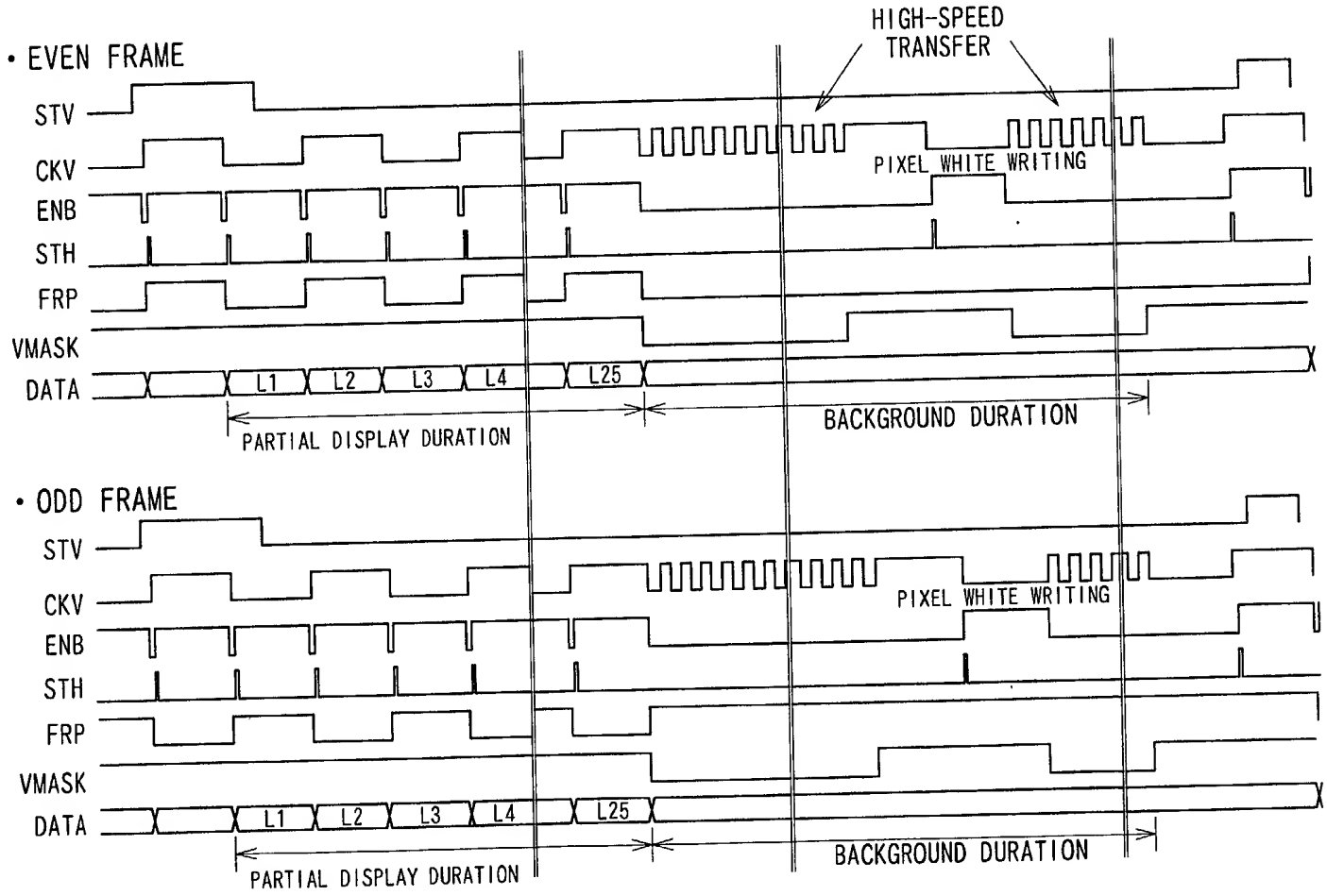
TIMING CHART IN NORMAL DISPLAY

FIG. 9



TIMING CHART IN BACKGROUND DISPLAY

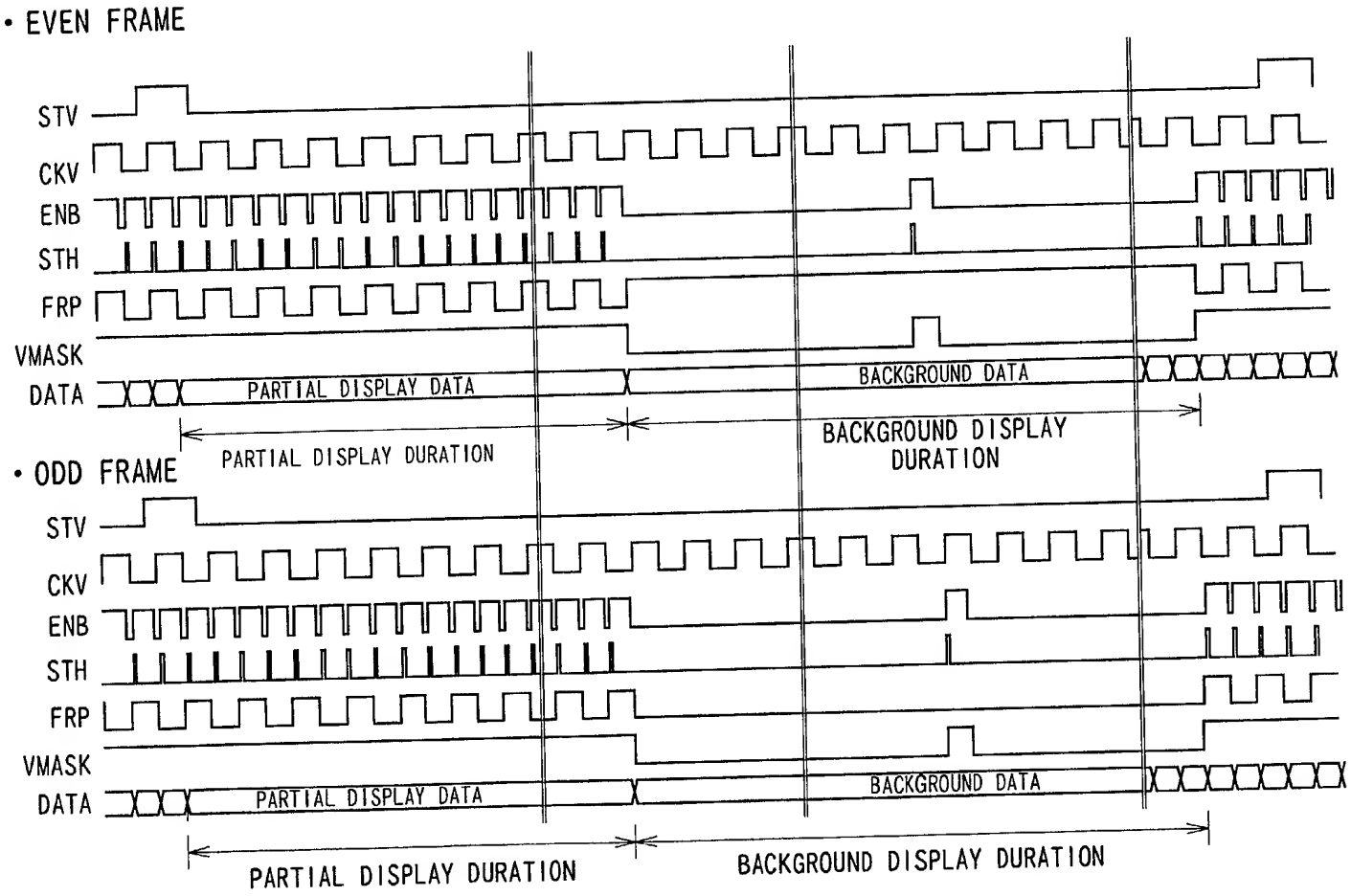
FIG. 10



TIMING CHART IN PARTIAL DISPLAY (DRIVING METHODS 1 AND 4)

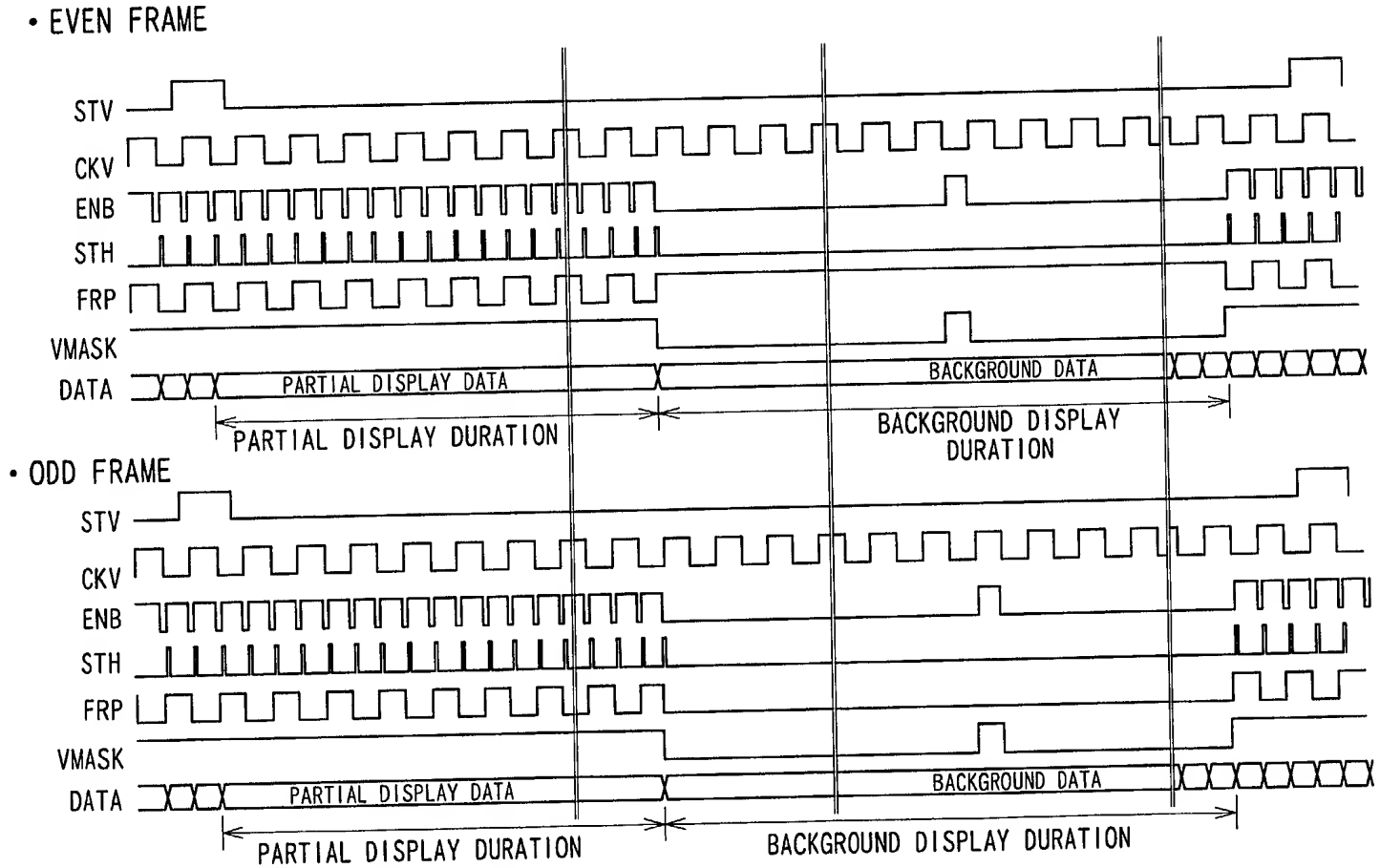
FIG. 11

EP 0 806 757 A2



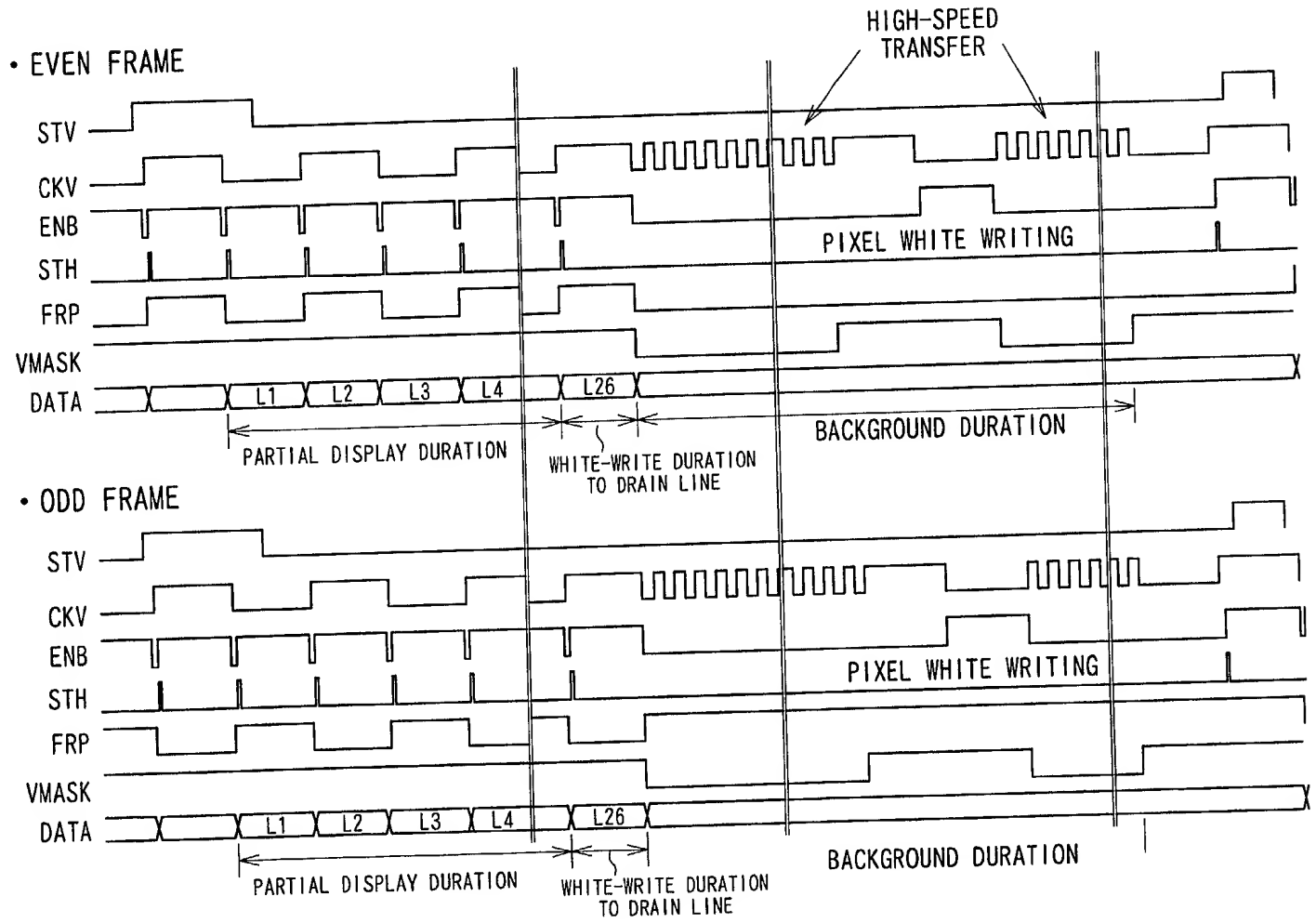
TIMING CHART IN PARTIAL DISPLAY (DRIVING METHOD 1)

FIG. 12



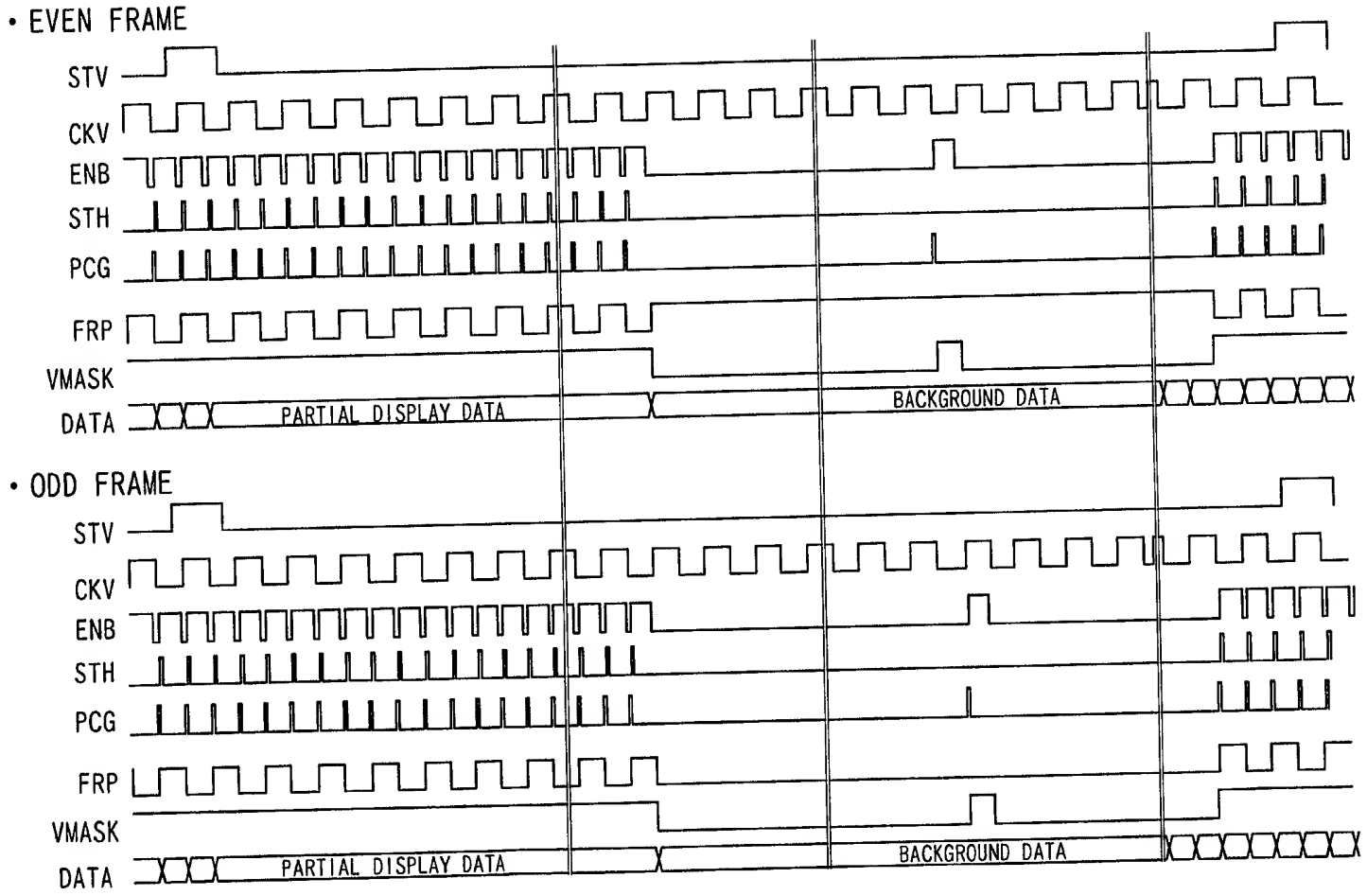
TIMING CHART IN PARTIAL DISPLAY (DRIVING METHOD 2)

FIG. 13



TIMING CHART IN PARTIAL DISPLAY (DRIVING METHODS 2 AND 4)

FIG. 14



TIMING CHART IN PARTIAL DISPLAY (DRIVING METHOD 3)

FIG. 15

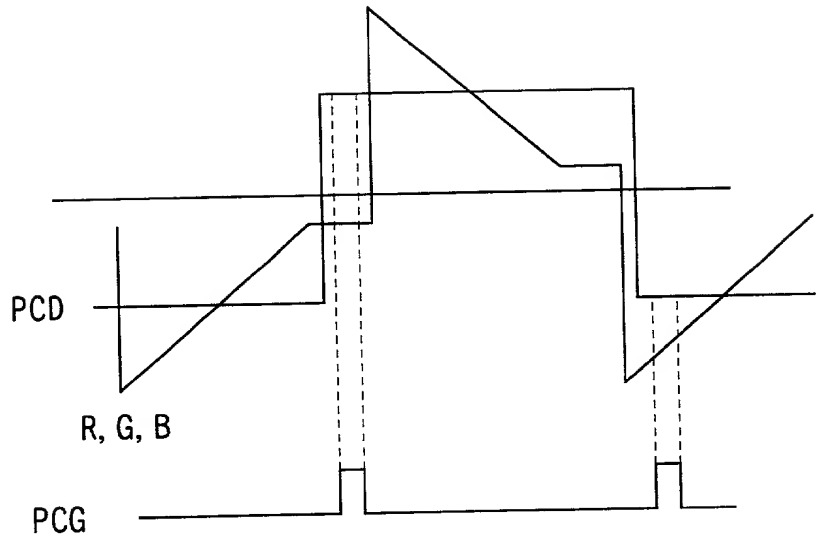
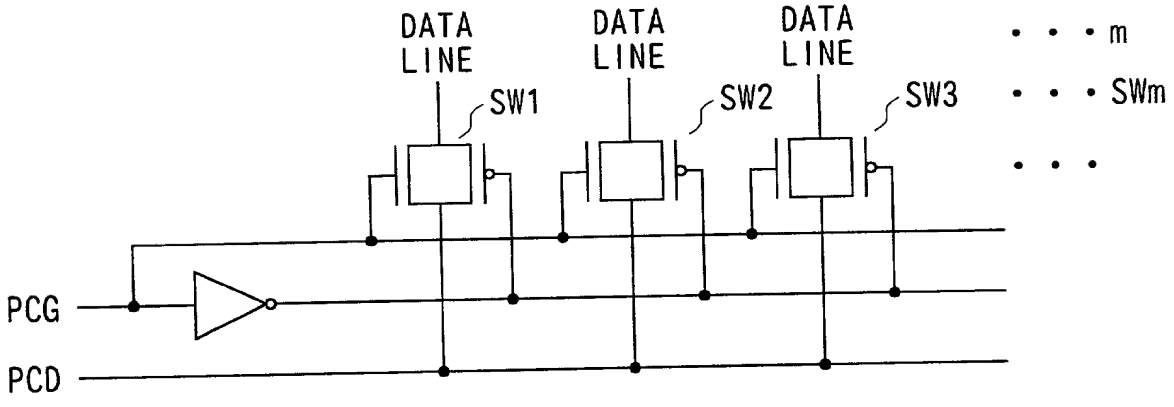
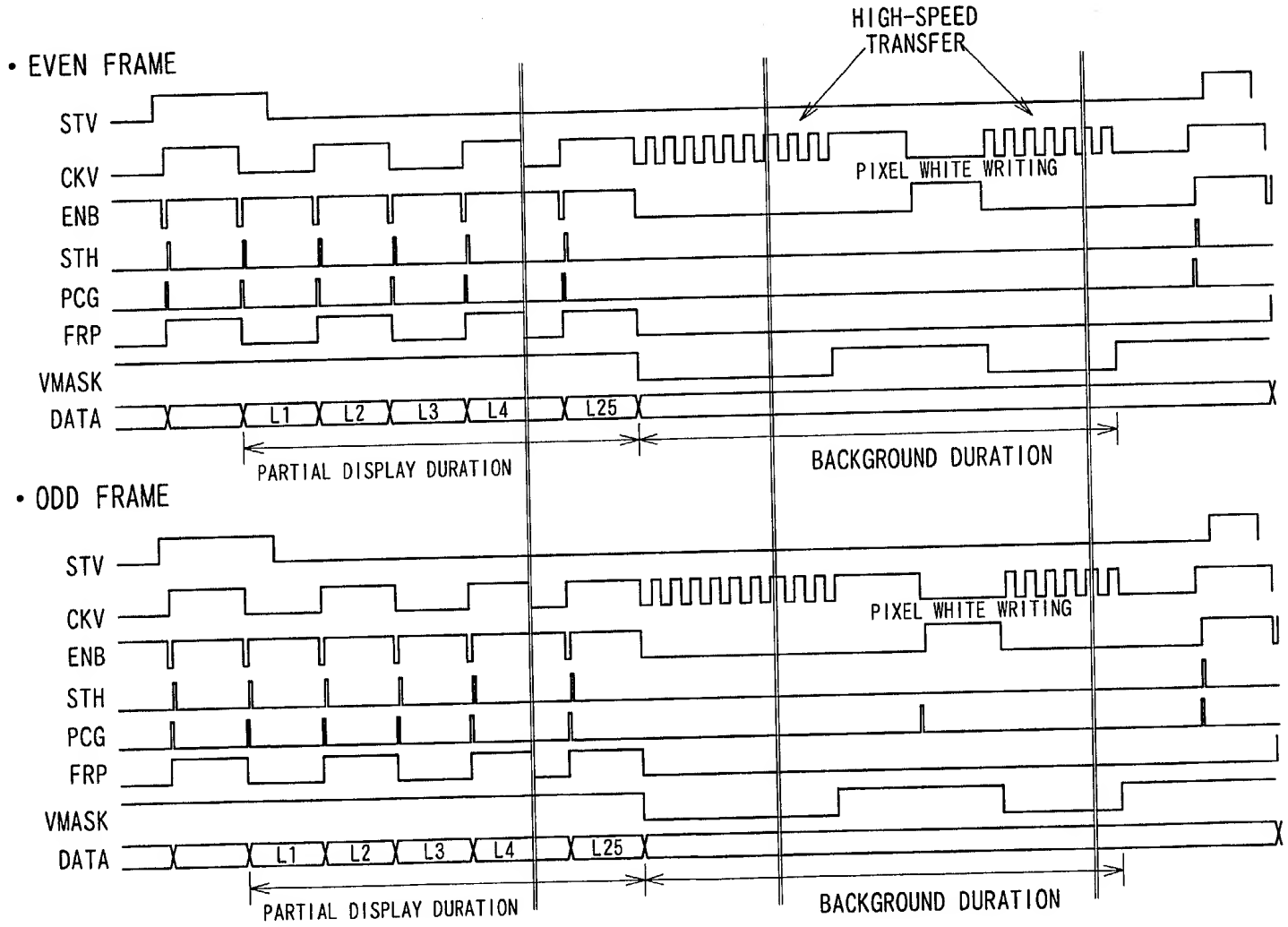


FIG. 16



230 : PRE-CHARGE DRIVER

FIG. 17



TIMING CHART IN PARTIAL DISPLAY (DRIVING METHODS 3 AND 4)

FIG. 18

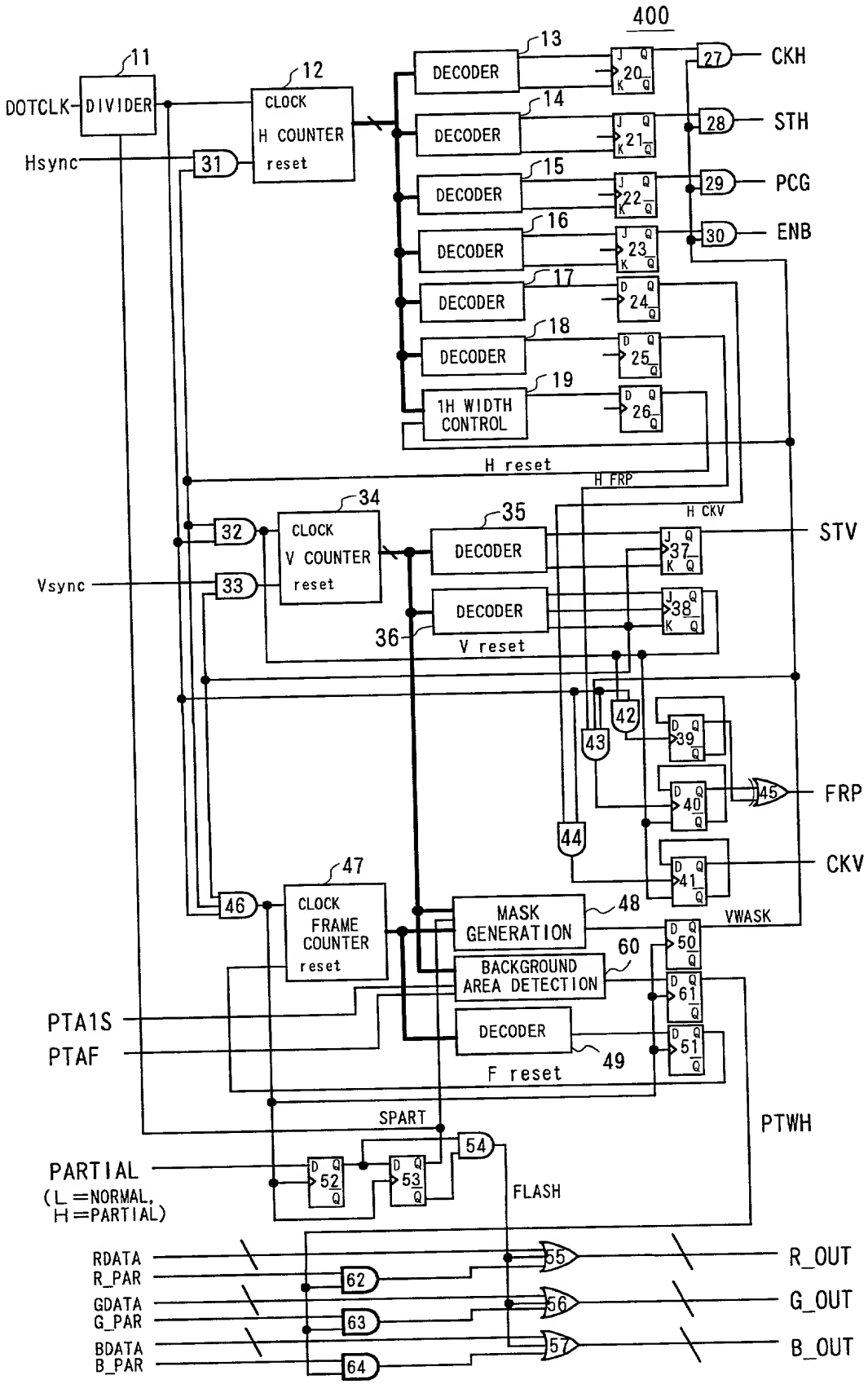
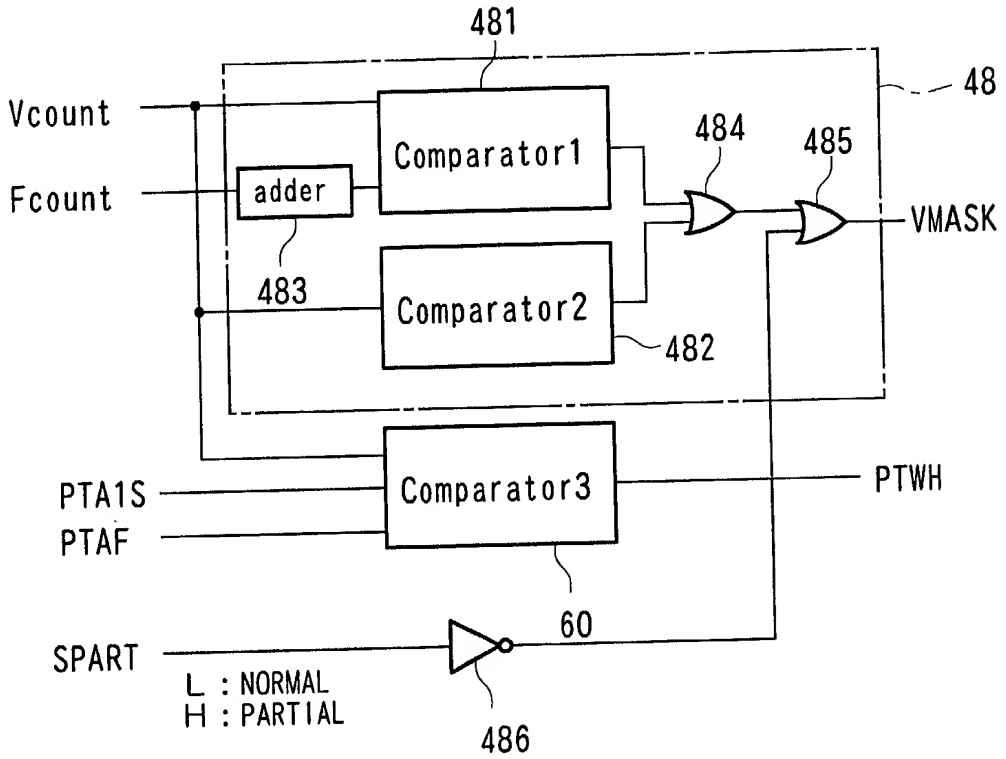

400
11
DIVIDER
DOTCLK
12
CLOCK
H COUNTER
reset
Hsync
31
DECODER
13
20
14
21
15
22
16
23
17
24
18
25
19
1H WIDTH
CONTROL
26
27
CKH
28
STH
29
PCG
30
ENB
H reset
H FRP
H CKV
34
CLOCK
V COUNTER
reset
32
Vsync
33
35
DECODER
37
STV
38
36
V reset
42
43
39
45
FRP
40
44
41
CKV
47
CLOCK
FRAME
COUNTER
reset
46
MASK
GENERATION
48
VWASK
50
60
BACKGROUND
AREA DETECTION
61
PTA1S
PTAF
DECODER
49
51
F reset
SPART
PTWH
54
PARTIAL
(L=NORMAL,
H=PARTIAL)
52
53
FLASH
RDATA
R_PAR
62
65
R_OUT
GDATA
G_PAR
63
66
G_OUT
BDATA
B_PAR
64
67
B_OUT

FIG. 19




```
Comparator3:if(PTAF=1)
              if(Vcount<25)      →Low
              else               →High
            elseif(Vcount<25)    →High
            else                 →Low
```

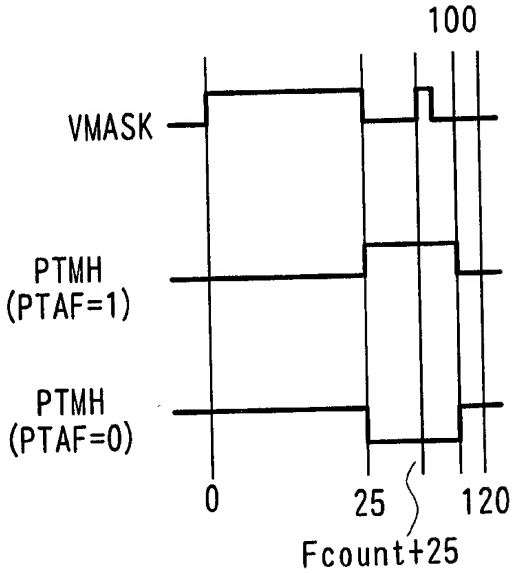


FIG. 20

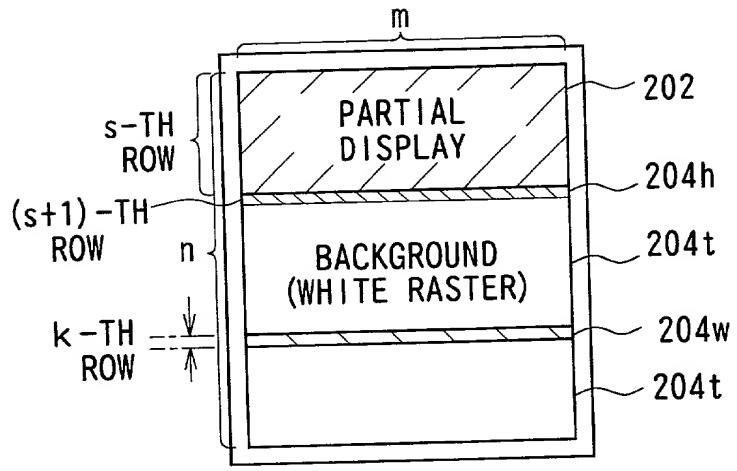

m
s-TH ROW
(s+1)-TH ROW
n
k-TH ROW
PARTIAL DISPLAY
BACKGROUND (WHITE RASTER)
202
204h
204t
204w
204t

FIG. 21

```
Comparator1:if(Vcount=fcount+25+1)→High
            else                  →Low


Comparator2:if(Vcount<25+1)→High
            else           →Low


Comparator3:if(PTAF=1)
              if(Vcount<25+1)   →Low
              else              →High
            elseif(Vcount<25)   →High
            else                →Low
```

FIG. 22

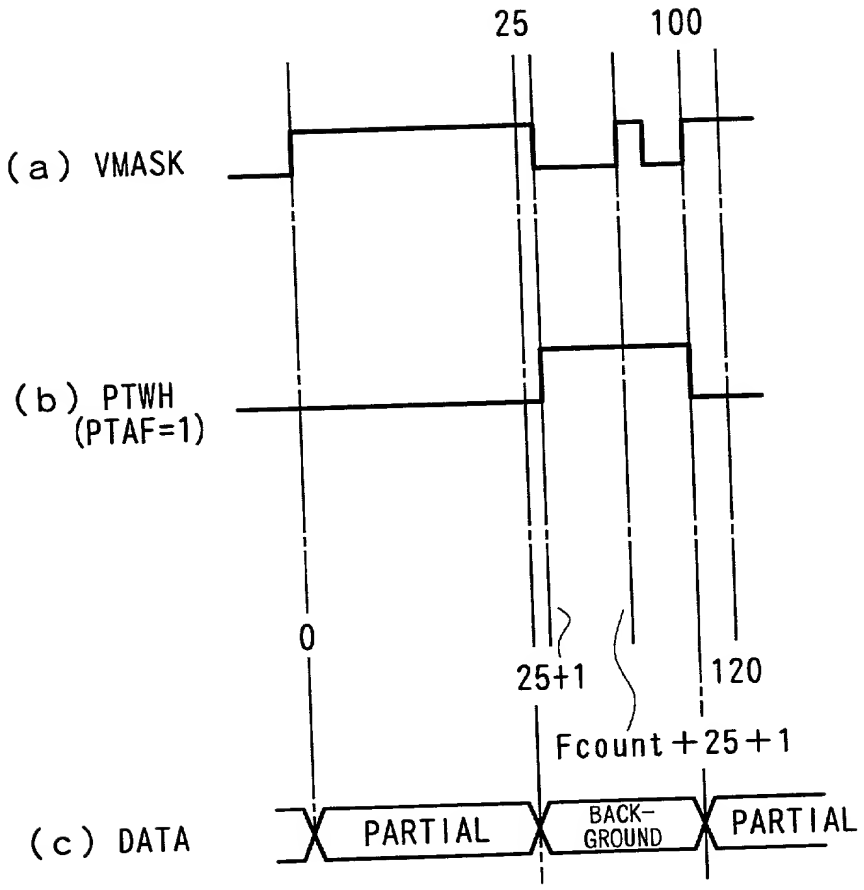

25
100
(a) VMASK
(b) PTWH
(PTAF=1)
0
25+1
120
Fcount+25+1
(c) DATA
PARTIAL
BACK-
GROUND
PARTIAL

FIG. 23

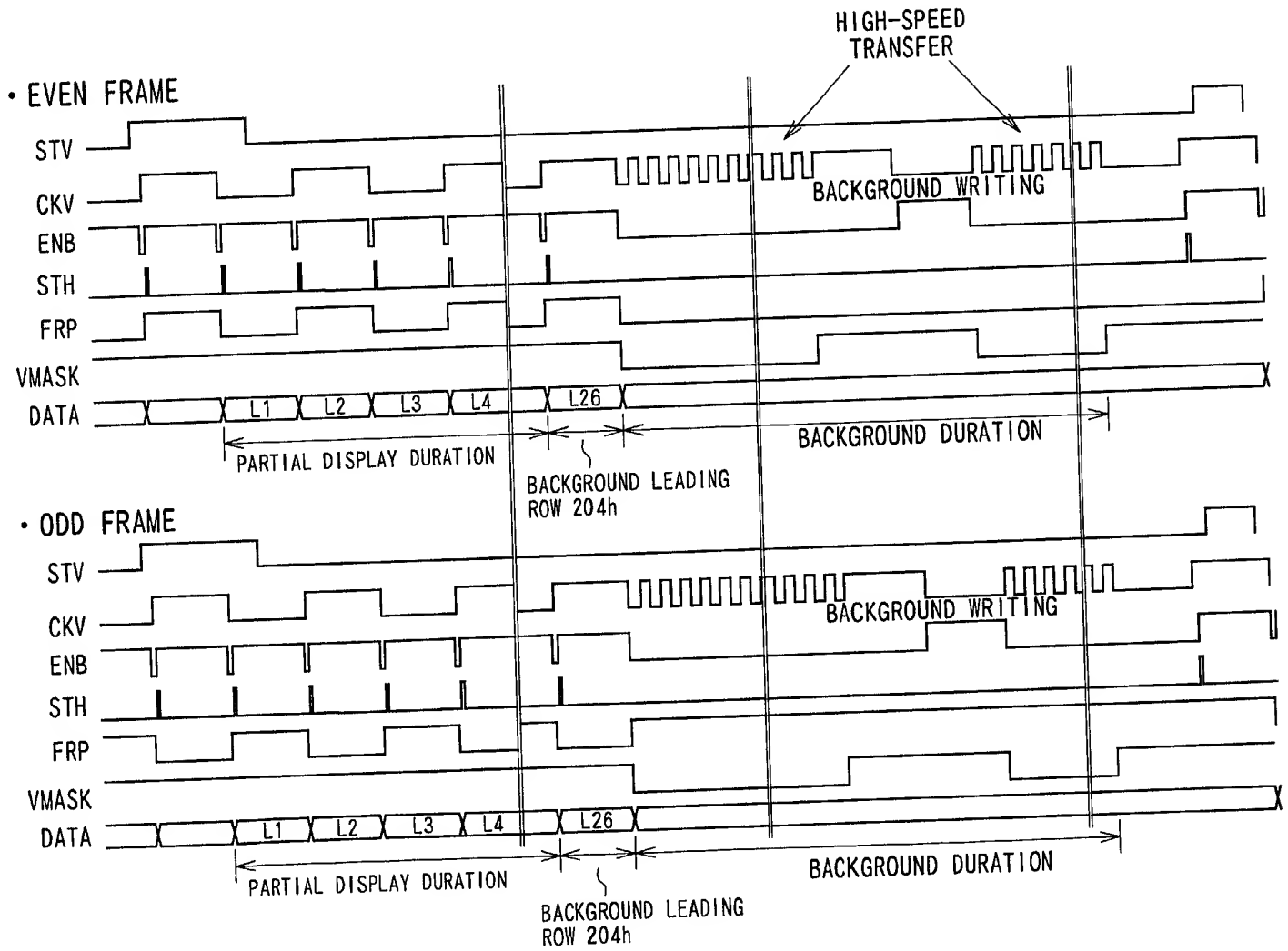

HIGH-SPEED TRANSFER
• EVEN FRAME
STV
CKV
ENB
STH
FRP
VMASK
DATA
L1
L2
L3
L4
L26
BACKGROUND WRITING
PARTIAL DISPLAY DURATION
BACKGROUND LEADING ROW 204h
BACKGROUND DURATION
• ODD FRAME
STV
CKV
ENB
STH
FRP
VMASK
DATA
L1
L2
L3
L4
L26
BACKGROUND WRITING
PARTIAL DISPLAY DURATION
BACKGROUND LEADING ROW 204h
BACKGROUND DURATION

FIG. 24

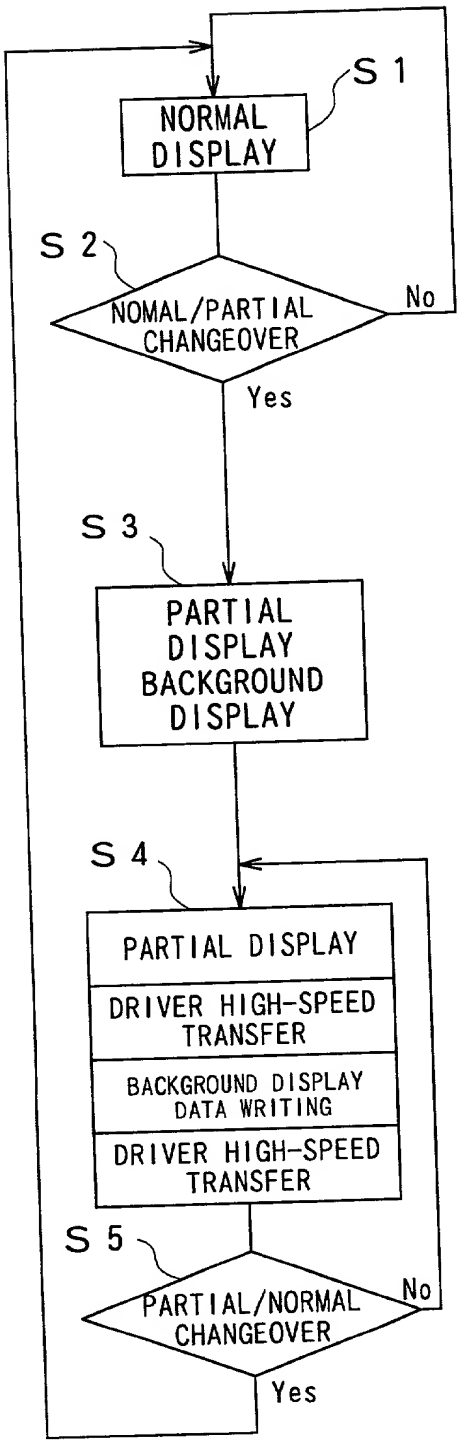


FIG. 25 (d)

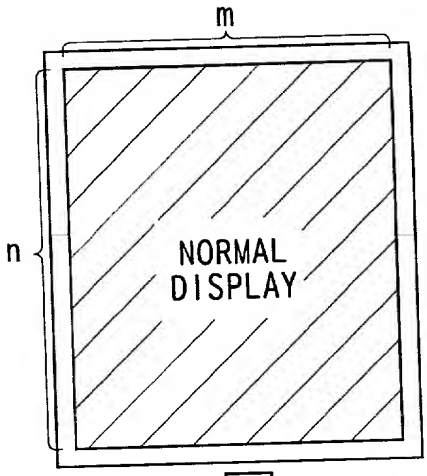


FIG. 25 (a)

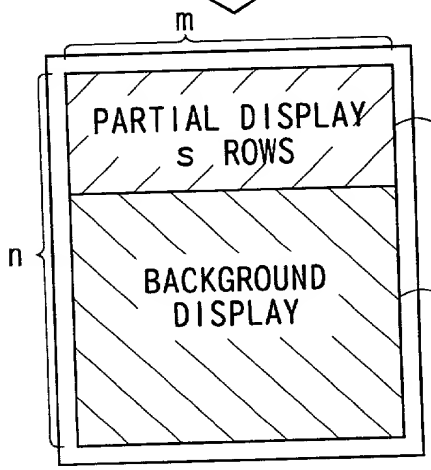


FIG. 25 (b)

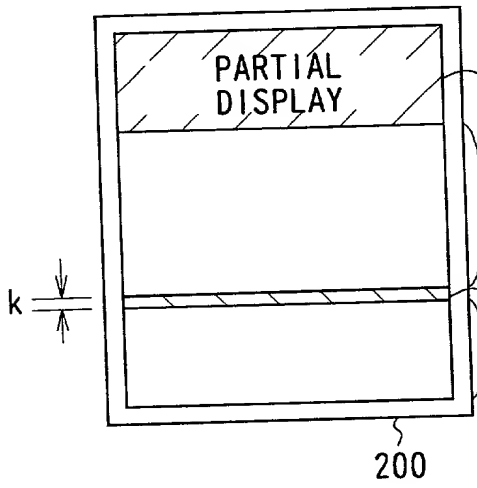


FIG. 25 (c)

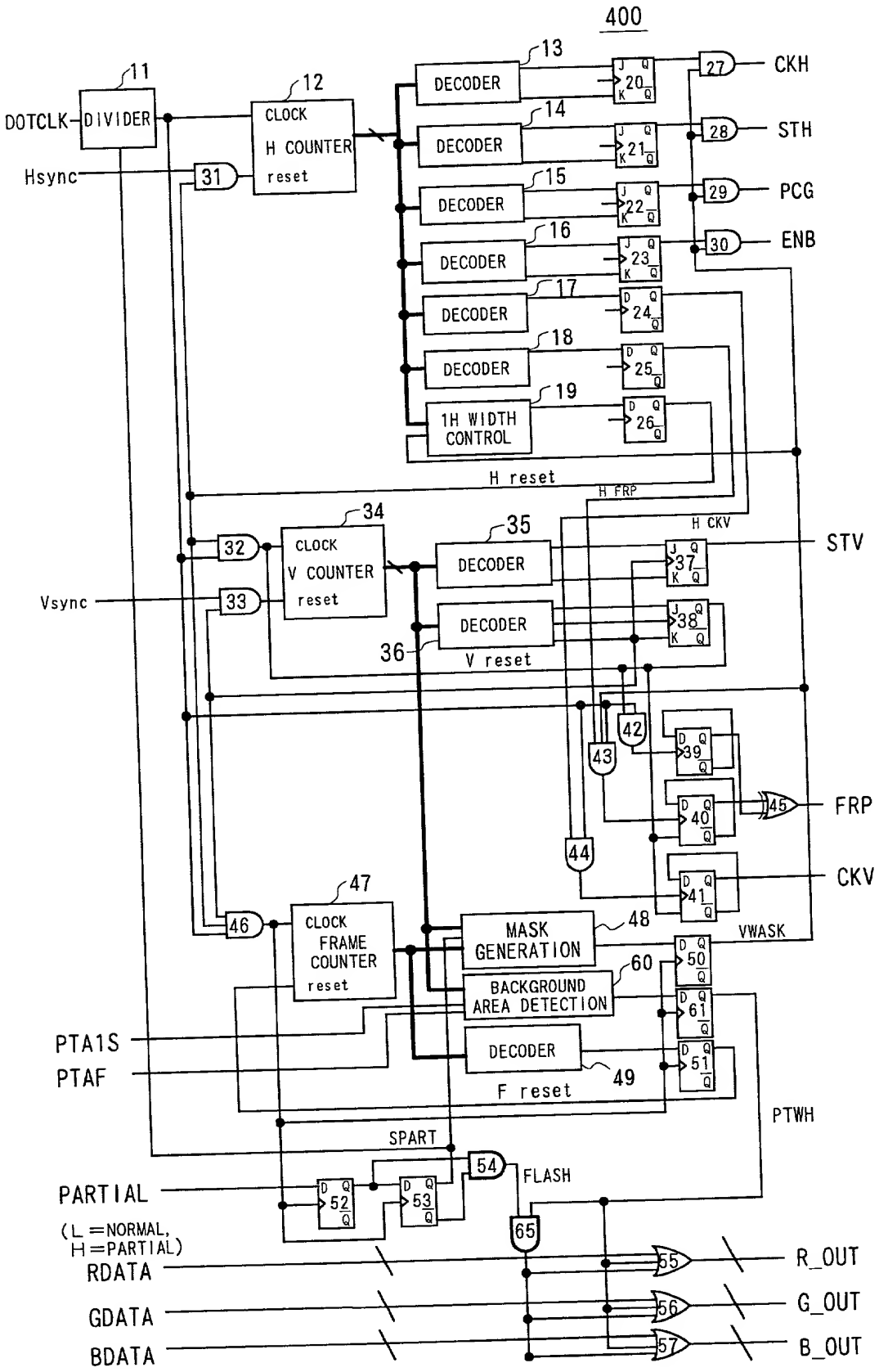

400
DOTCLK
DIVIDER
11
12
CLOCK
H COUNTER
reset
Hsync
31
DECODER
13
14
15
16
17
18
19
1H WIDTH
CONTROL
20
21
22
23
24
25
26
27
28
29
30
CKH
STH
PCG
ENB
H reset
H FRP
H CKV
STV
34
CLOCK
V COUNTER
reset
32
33
Vsync
35
36
V reset
37
38
42
43
44
39
40
41
45
FRP
CKV
46
47
CLOCK
FRAME
COUNTER
reset
MASK
GENERATION
48
VWASK
BACKGROUND
AREA DETECTION
60
50
61
51
PTA1S
PTAF
DECODER
49
F reset
PTWH
SPART
54
FLASH
PARTIAL
(L=NORMAL,
H=PARTIAL)
52
53
65
RDATA
GDATA
BDATA
55
56
57
R_OUT
G_OUT
B_OUT

FIG. 26